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The receiver features a variable-gain amplifier (VGA), DFE, and ... The VGA drives a second-stage peaking amplifier that is used to ...
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Variable gain amplifier - Patent # 7250814 - PatentGenius
A method of varying the gain of an amplifier and an amplifier array are provided. The amplifier array includes two or more amplifier stages (201, ...
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The receiver features a variable-gain amplifier (VGA) with gain ranging from -6 to +10 dB in ~1 dB steps, an analog peaking amplifier, and a continuously ...
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High Speed Multi-Mode Receiver - Patent 20060067440
The receiver is further operable to perform adaptive equalization to ... gain control unit includes a variable gain amplifier and a peaking amplifier, ...
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Hui Dong Lee; Kyung Ai Lee; Songcheol Hong;
Microwave Theory and Techniques, IEEE Transactions on
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10. Adaptive signal processing with genetic algorithm optimum filter for fas
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...problems of equalization and noise...FIG. 1A, an equalizati
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This invention provides a signal processing and signal synthesis signal processing and signal synthesis techniques designed to re individually in creating new forms of rich musical timbres. Synth
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9. Derivation of control signals from real-time overtone measurem
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A system for control signal generation using detected dynamic c components of an incoming electronic signal. Fixed or adjustable coupled to signal parameter measurement elements. Each filter
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UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT
patno:US20060067440
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Caresosa, Mario / Yin, Guangming, *UNITED STATES PATENT PRE-GRANT PUBLICATION*, Mar 2007
patno:US20070069817
...produces an output swing that is equal to a pre-determined a required...coupled to a supply voltage VDD via shunt peaking ir respectively...a more complicated task. Because of distortion c range of...the Vc approaches the region where the distortion st the high...should be at a Vc that represents some pre-determin amplification...
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...produces an output swing that is equal to a pre-determined a required...coupled to a supply voltage VDD via shunt peaking ir respectively...a more complicated task. Because of distortion c range of...the Vc approaches the region where the distortion st the high...should be at a Vc that represents some pre-determin amplification...
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3. Adaptable voltage control for a variable gain amplifier
Caresosa, Mario / Yin, Guangming (Broadcom Corporatior *PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Nov 2006
patno:US7135926
...produces an output swing that is equal to a pre-determined a required...coupled to a supply voltage VDD via shunt peaking ir respectively...a more complicated task. Because of distortion c range of...the Vc approaches the region where the distortion st the high...should be at a Vc that represents some pre-determin amplification...
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4. Adaptable voltage control for a variable gain amplifier
Caresosa, Mario / Yin, Guangming (BROADCOM CORPORA *PATENT AND TRADEMARK OFFICE PRE-GRANT PUBLICATION*, Fe
patno:US20060028270
...produces an output swing that is equal to a pre-determined a required...coupled to a supply voltage VDD via shunt peaking ir respectively...a more complicated task. Because of distortion c range of...the Vc approaches the region where the distortion st the high...should be at a Vc that represents some pre-determin amplification...
Full text available at patent office. For more in-depth sear
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5. ADAPTABLE VOLTAGE CONTROL FOR A VARIABLE GAIN AMPLIFI
Caresosa, Mario / Yin, Guangming, *UNITED STATES PATENT PRE-GRANT PUBLICATION*, Nov 2005
patno:US20050258900
...produces an output swing that is equal to a pre-determined a required...coupled to a supply voltage VDD via shunt peaking ir respectively...a more complicated task. Because of distortion c range of...the Vc approaches the region where the distortion st

the high...should be at a Vc that represents some pre-determin
amplification...
Full text available at patent office. For more in-depth sear
similar results

6. Adaptable voltage control for a variable gain amplifier
Caresosa, Mario / Yin, Guangming (Broadcom Corporatior
PATENT AND TRADEMARK OFFICE GRANTED PATENT, Dec 2005
patno:US6980053
...produces an output swing that is equal to a pre-determined a
required...coupled to a supply voltage VDD via shunt peaking ir
respectively...a more complicated task. Because of distortion c
range of...the Vc approaches the region where the distortion st
the high...should be at a Vc that represents some pre-determin
amplification...
Full text available at patent office. For more in-depth sear
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7. High Speed Multi-Mode Receiver
Hsu, Louis C. / Ji, Brian L. / Mason, James S. / Selander, I
A. / Zier, Steven J. (INTERNATIONAL BUSINESS MACHINE
UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT
patno:US20060067440
...invention includes a central equalization unit operable to ger
the equalization information may include...another embodimer
information may include...the DFE to compensate distortion. To
unit 62 includes a variable gain amplifier (VGA) 310, a peaki
offset...
Full text available at patent office. For more in-depth sear
similar results

8. Reconfigurable Equalization for 10-Gb/sec Serial Data Links in a
Technology
BIEN, FRANKLIN YOUNG-JAE , Nov 2006
Reconfigurable Equalization for 10-Gb/sec Serial...VARIABLE T
AMPLIFIER...Output Monitoring VGA Variable Gain Amplifier
Gain...using electrical equalization implemented in an...
Full text thesis available via NDLTD (Georgia Tech)
similar results

9. Chip equalization and transmit antenna diversity for high-speed
Meshkati, Farhad , Jan 2001
...noise low- distortion switchable-gain amplifier, and a low...
amplifier...a filter: a variable gain amplifier, and a set...by n
verification...switched gain amplifiers and the variable gain a
determine...noise figure, distortion, dynamic range...
Full text thesis available via NDLTD (Library and Archives
similar results

10. Adaptive noise filtering and equalization for optimal high speed
Kim, Andrew Joo / Hietala, Vincent Mark / Bajekal, Sanja
UNITED STATES PATENT AND TRADEMARK OFFICE PRE-GRANT
patno:US20060239390
...problems of equalization and noise filtering...comprise a var
105, a signal...particular type of distortion using a relatively...
amplifier 105, and filter...the signal be pre-filtered with...T0) a
with gain...help improve equalization. Filtering...Removing the
transmission...distortions, but also pre-compensates...
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Application Number Information

Application Number: 10/711713
Assignments

Examiner Number: 80488 / TORRES, JUAN

Filing or 371(c) Date: 09/30/2004 eDan

Group Art Unit: 2611 IFW Madras

Effective Date: 09/30/2004

Class/Subclass: 375/345.000

Application Received: 09/30/2004

Lost Case: NO

Waiting for Response Desc.
Mail Non Final

Pat. Num./Pub. Num: /20060067440

Interference Number:

Issue Date: 00/00/0000

Unmatched Petition: NO

Date of Abandonment: 00/00/0000

L&R Code: Secrecy Code:1

Attorney Docket Number: FIS920040082US1

Third Level Review: NO

Secrecy Order: NO

Status: 41 /NON FINAL ACTION MAILED

Status Date: 12/10/2007

Confirmation Number: 5712

Oral Hearing: NO

Title of Invention: HIGH SPEED MULTI-MODE RECEIVER

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IDS Flag Clearance for Application 10711713

IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
WIDS	2004-10-18	23	Y ☑	2007-09-04 22:10:27.0	jtorres1

Update

Inventor Information for 10/711713

Inventor Name	City	State/Country
HSU, LOUIS C.	FISHKILL	NEW YORK
JI, BRIAN L.	FISHKILL	NEW YORK
MASON, JAMES S.	EASTLEIGH	UNITED KINGDOM
SELANDER, KARL D.	HOPEWELL JUNCTION	NEW YORK
SORNA, MICHAEL A.	HOPEWELL JUNCTION	NEW YORK
ZIER, STEVEN J.	HOPEWELL JUNCTION	NEW YORK

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Inventor Name Search Result

Your Search was:

Last Name = JI
First Name = BRIAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09257146	6477630	150	02/24/1999	HIERARCHICAL ROW ACTIVATION METHOD FOR BANKING CONTROL IN MULTI-BANK DRAM	JI, BRIAN
09333539	6081479	150	06/15/1999	HIERARCHICAL PREFETCH FOR SEMICONDUCTOR MEMORIES	JI, BRIAN
09579749	6252806	150	05/26/2000	Multi-generator, partial array Vt tracking system to improve array retention time	JI, BRIAN L.
09712628	6400639	150	11/14/2000	WORDLINE DECODER SYSTEM AND METHOD	JI, BRIAN L.
10063466	6801980	150	04/25/2002	DESTRUCTIVE-READ RANDOM ACCESS MEMORY SYSTEM BUFFERED WITH DESTRUCTIVE-READ MEMORY CACHE	JI, BRIAN L.
10145018	7216284	150	05/15/2002	CONTENT ADDRESSABLE MEMORY HAVING REDUCED POWER CONSUMPTION	JI, BRIAN L.
10249546	6980824	150	04/17/2003	METHOD AND SYSTEM FOR OPTIMIZING TRANSMISSION AND RECEPTION POWER LEVELS IN A COMMUNICATION SYSTEM	JI, BRIAN L.
10314497	Not Issued	161	12/06/2002	Apparatus and method for shielding a wafer from charged particles during plasma etching	JI, BRIAN L.
10320842	Not Issued	161	12/16/2002	Magnetic mirror for preventing wafer edge damage during dry etching	JI, BRIAN L.
10334312	6823293	150	12/31/2002	HIERARCHICAL POWER SUPPLY NOISE MONITORING DEVICE AND SYSTEM FOR VERY LARGE SCALE INTEGRATED CIRCUITS	JI, BRIAN L.
10673801	7355872	150	09/29/2003	SEGMENTED CONTENT ADDRESSABLE MEMORY	JI, BRIAN L.

				ARCHITECTURE FOR IMPROVED CYCLE TIME AND REDUCED POWER CONSUMPTION	
10707199	6975140	150	11/26/2003	ADAPTIVE DATA TRANSMITTER HAVING REWRITEABLE NON-VOLATILE STORAGE	JI, BRIAN L.
10710169	6948028	150	06/23/2004	DESTRUCTIVE-READ RANDOM ACCESS MEMORY SYSTEM BUFFERED WITH DESTRUCTIVE-READ MEMORY CACHE	JI, BRIAN L.
10711713	Not Issued	41	09/30/2004	High Speed Multi-Mode Receiver	JI, BRIAN L.
10993941	7005319	150	11/19/2004	GLOBAL PLANARIZATION OF WAFER SCALE PACKAGE WITH PRECISION DIE THICKNESS CONTROL	JI, BRIAN L.
10996312	Not Issued	93	11/23/2004	ON-CHIP ELECTRICALLY ALTERABLE RESISTOR	JI, BRIAN L.
11098078	7233177	150	04/04/2005	PRECISION TUNING OF A PHASE-CHANGE RESISTIVE ELEMENT	JI, BRIAN L.
11160220	7203794	150	06/14/2005	DESTRUCTIVE-READ RANDOM ACCESS MEMORY SYSTEM BUFFERED WITH DESTRUCTIVE-READ MEMORY CACHE	JI, BRIAN L.
11172473	7319608	150	06/30/2005	NON-VOLATILE CONTENT ADDRESSABLE MEMORY USING PHASE-CHANGE-MATERIAL MEMORY ELEMENTS	JI, BRIAN L.
11193878	Not Issued	41	07/29/2005	Write operations for phase-change-material memory	JI, BRIAN L.
11260375	Not Issued	41	10/28/2005	Apparatus and method for shielding a wafer from charged particles during plasma etching	JI, BRIAN L.
11297730	7342406	150	12/08/2005	METHODS AND APPARATUS FOR INLINE VARIABILITY MEASUREMENT OF INTEGRATED CIRCUIT COMPONENTS	JI, BRIAN L.
11623434	Not Issued	41	01/16/2007	Multi-Port Dynamic Memory Structures	JI, BRIAN L.
11929943	Not Issued	20	10/30/2007	Embedded DRAM Integrated Circuits With Extremely Thin Silicon-On-Insulator Pass Transistors	JI, BRIAN L.

12041388	Not Issued	17	03/03/2008	Methods and Apparatus for Inline Variability Measurement of Integrated Circuit Components	JI, BRIAN L.
60119713	Not Issued	159	02/11/1999	HIERARCHICAL PREFETCH FOR SEMICONDUCTOR MEMORIES	JI, BRIAN L.
10688744	Not Issued	161	10/17/2003	Output driver impedance control for addressable memory devices	JI, BRIAN LI
09419594	Not Issued	164	10/18/1999	ADDRESS WRAP FUNCTION FOR ADDRESSABLE MEMORY DEVICES	JI, BRIAN LI
11322330	Not Issued	30	12/30/2005	Multi-unit condominium structure using foundation zones	JIMENEZ, BRIAN R.
11322380	Not Issued	30	12/30/2005	Multi-unit condominium structure with configurable space designs	JIMENEZ, BRIAN R.
11323891	Not Issued	30	12/30/2005	Method of constructing and selling condominium units	JIMENEZ, BRIAN R.
11936966	Not Issued	25	11/08/2007	IDENTITY MANAGEMENT SUITE	JIMERSON, BRIAN
09491763	Not Issued	161	01/27/2000	Collapsible sports goal	JIRSA, BRIAN

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Inventor Name Search Result

Your Search was:

Last Name = SELANDER
First Name = KARL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09761049	6356114	150	01/16/2001	High speed receiver with integrated CMOS and PECL capability	SELANDER, KARL
10249545	6891357	150	04/17/2003	REFERENCE CURRENT GENERATION SYSTEM AND METHOD	SELANDER, KARL D.
10249546	6980824	150	04/17/2003	METHOD AND SYSTEM FOR OPTIMIZING TRANSMISSION AND RECEPTION POWER LEVELS IN A COMMUNICATION SYSTEM	SELANDER, KARL D.
10249795	6680681	150	05/08/2003	HIGH SPEED FIR TRANSMITTER	SELANDER, KARL D.
10250043	6937054	150	05/30/2003	PROGRAMMABLE PEAKING RECEIVER AND METHOD	SELANDER, KARL D.
10604025	7352815	150	06/23/2003	DATA TRANSCEIVER AND METHOD FOR EQUALIZING THE DATA EYE OF A DIFFERENTIAL INPUT DATA SIGNAL	SELANDER, KARL D.
10710064	7295618	150	06/16/2004	AUTOMATIC ADAPTIVE EQUALIZATION METHOD AND SYSTEM FOR HIGH-SPEED SERIAL TRANSMISSION LINK	SELANDER, KARL D.
10711713	Not Issued	41	09/30/2004	High Speed Multi-Mode Receiver	SELANDER, KARL D.
10905436	7205830	150	01/04/2005	ANALOG MOS CIRCUITS HAVING REDUCED VOLTAGE STRESS	SELANDER, KARL D.
10905704	7102392	150	01/18/2005	IMPROVED SIGNAL DETECTOR FOR HIGH-SPEED SERDES	SELANDER, KARL D.
10905705	Not Issued	41	01/18/2005	FRONT END INTERFACE FOR DATA RECEIVER	SELANDER, KARL D.
10908959	Not Issued	30	06/02/2005	APPARATUS AND METHOD FOR REDUCED LOADING OF SIGNAL TRANSMISSION	SELANDER, KARL D.

				ELEMENTS	
11103314	7132821	150	04/11/2005	REFERENCE CURRENT GENERATION SYSTEM	SELANDER, KARL D.
11163688	7332956	150	10/27/2005	METHOD TO AVOID DEVICE STRESSING	SELANDER, KARL D.
11383821	Not Issued	41	05/17/2006	Signal Detector with Calibration Circuit Arrangement	SELANDER, KARL D.
11964894	Not Issued	19	12/27/2007	AVOIDING DEVICE STRESSING	SELANDER, KARL D.
11974967	Not Issued	17	10/17/2007	Automatic adaptive equalization method for high-speed serial transmission link	SELANDER, KARL D.
11999627	Not Issued	19	12/06/2007	Design structure for apparatus for reduced loading of signal transmission elements	SELANDER, KARL D.
09017719	5825169	250	02/04/1998	DYNAMICALLY BIASED CURRENT GAIN VOLTAGE REGULATOR WITH LOW QUIESCENT POWER CONSUMPTION	SELANDER, KARL D.
10915790	Not Issued	93	08/11/2004	METHODS AND ARRANGEMENTS FOR LINK POWER REDUCTION	SELANDER, KARL DAVID
10994742	Not Issued	41	11/22/2004	Timing bias compensation for a data receiver with decision-feedback equalizer	SELANDER, KARL DAVID
06279591	4423571	150	07/01/1981	QUICK CHANGE SHOE ASSEMBLY FOR STRAIGHT LINE SANDER	SELANDER, KARL W.

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Inventor Name Search Result

Your Search was:

Last Name = SORNA
First Name = MICHAEL

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09757107	6466100	150	01/08/2001	LINEAR VOLTAGE CONTROLLED OSCILLATOR TRANSCONDUCTOR WITH GAIN COMPENSATION	SORNA, MICHAEL A.
09761526	6528777	150	01/16/2001	OPTICAL POWER METER DERIVED FROM COMMON-MODE VOLTAGE OF OPTICAL TRANSIMPEDANCE AMPLIFIER	SORNA, MICHAEL A.
09887792	6785832	150	06/22/2001	PROCESS INDEPENDENT SOURCE SYNCHRONOUS DATA CAPTURE APPARATUS AND METHOD	SORNA, MICHAEL A.
10064387	7321617	150	07/09/2002	DATA COMMUNICATION SYSTEM WITH SELF-TEST FEATURE	SORNA, MICHAEL A.
10139931	6661267	150	05/06/2002	COARSE CALIBRATION CIRCUIT USING VARIABLE STEP SIZES TO REDUCE JITTER AND A DYNAMIC COURSE CALIBRATION (DCC) CIRCUIT FOR A 2 GHZ VCO	SORNA, MICHAEL A.
10160541	7142623	150	05/31/2002	ON-CHIP SYSTEM AND METHOD FOR MEASURING JITTER TOLERANCE OF A CLOCK AND DATA RECOVERY CIRCUIT	SORNA, MICHAEL A.
10249545	6891357	150	04/17/2003	REFERENCE CURRENT GENERATION SYSTEM AND METHOD	SORNA, MICHAEL A.
10249546	6980824	150	04/17/2003	METHOD AND SYSTEM FOR OPTIMIZING TRANSMISSION AND RECEPTION POWER LEVELS IN A COMMUNICATION SYSTEM	SORNA, MICHAEL A.
10249795	6680681	150	05/08/2003	HIGH SPEED FIR TRANSMITTER	SORNA, MICHAEL A.
10250043	6937054	150	05/30/2003	PROGRAMMABLE PEAKING RECEIVER AND METHOD	SORNA, MICHAEL A.

10604025	7352815	150	06/23/2003	DATA TRANSCEIVER AND METHOD FOR EQUALIZING THE DATA EYE OF A DIFFERENTIAL INPUT DATA SIGNAL	SORNA, MICHAEL A.
10604419	7113749	150	07/18/2003	SYSTEM AND METHOD FOR MEASURING A HIGH SPEED SIGNAL	SORNA, MICHAEL A.
10707123	6956417	150	11/21/2003	LEAKAGE COMPENSATION CIRCUIT	SORNA, MICHAEL A.
10707171	6963240	150	11/25/2003	DAMPING OF LC RINGING IN IC (INTEGRATED CIRCUIT) POWER DISTRIBUTION SYSTEMS	SORNA, MICHAEL A.
10708233	6949981	150	02/18/2004	DYNAMIC THRESHOLD FOR VCO CALIBRATION	SORNA, MICHAEL A.
10710064	7295618	150	06/16/2004	AUTOMATIC ADAPTIVE EQUALIZATION METHOD AND SYSTEM FOR HIGH-SPEED SERIAL TRANSMISSION LINK	SORNA, MICHAEL A.
10710745	7053712	150	07/30/2004	METHOD AND APPARATUS FOR CONTROLLING COMMON-MODE OUTPUT VOLTAGE IN FULLY DIFFERENTIAL AMPLIFIERS	SORNA, MICHAEL A.
10711713	Not Issued	41	09/30/2004	High Speed Multi-Mode Receiver	SORNA, MICHAEL A.
10905704	7102392	150	01/18/2005	IMPROVED SIGNAL DETECTOR FOR HIGH-SPEED SERDES	SORNA, MICHAEL A.
10905705	Not Issued	41	01/18/2005	FRONT END INTERFACE FOR DATA RECEIVER	SORNA, MICHAEL A.
10908959	Not Issued	30	06/02/2005	APPARATUS AND METHOD FOR REDUCED LOADING OF SIGNAL TRANSMISSION ELEMENTS	SORNA, MICHAEL A.
10994742	Not Issued	41	11/22/2004	Timing bias compensation for a data receiver with decision-feedback equalizer	SORNA, MICHAEL A.
11103314	7132821	150	04/11/2005	REFERENCE CURRENT GENERATION SYSTEM	SORNA, MICHAEL A.
11306985	Not Issued	60	01/18/2006	ON-CHIP ELECTROMIGRATION MONITORING SYSTEM	SORNA, MICHAEL A.
11383821	Not Issued	41	05/17/2006	Signal Detector with Calibration Circuit Arrangement	SORNA, MICHAEL A.
11467349	Not Issued	41	08/25/2006	CML TO CMOS SIGNAL CONVERTER	SORNA, MICHAEL A.
11557676	Not	30	11/08/2006	Systems and Arrangements for	SORNA, MICHAEL

	Issued			Controlling an Impedance on a Transmission Path	A.
11759396	Not Issued	25	06/07/2007	OUT OF BAND SIGNALING ENHANCEMENT FOR HIGH SPEED SERIAL DRIVER	SORNA, MICHAEL A.
11766268	Not Issued	30	06/21/2007	Robust Cable Connectivity Test Receiver For High-Speed Data Receiver	SORNA, MICHAEL A.
11846581	Not Issued	30	08/29/2007	Data Communication System with Self-Test Feature	SORNA, MICHAEL A.
11968872	Not Issued	17	01/03/2008	SYSTEM FOR MEASURING AN EYEWIDTH OF A DATA SIGNAL IN AN ASYNCHRONOUS SYSTEM	SORNA, MICHAEL A.
11974967	Not Issued	17	10/17/2007	Automatic adaptive equalization method for high-speed serial transmission link	SORNA, MICHAEL A.
11985956	Not Issued	19	11/19/2007	Structure for robust cable connectivity test receiver for high-speed data receiver	SORNA, MICHAEL A.
11985966	Not Issued	25	11/19/2007	Design structure for on-chip electromigration monitoring system	SORNA, MICHAEL A.
11999627	Not Issued	19	12/06/2007	Design structure for apparatus for reduced loading of signal transmission elements	SORNA, MICHAEL A.
07620973	5132613	150	11/30/1990	LOW INDUCTANCE SIDE MOUNT DECOUPLING TEST STRUCTURE	SORNA, MICHAEL A.
07690404	5144228	150	04/23/1991	PROBE INTERFACE ASSEMBLY	SORNA, MICHAEL A.
08534900	5661395	250	09/28/1995	ACTIVE, LOW VSD, FIELD EFFECT TRANSISTOR CURRENT SOURCE	SORNA, MICHAEL A.
08884117	5912928	150	06/27/1997	HIGH SPEED SERIAL DATA TRANSMISSION ENCODER	SORNA, MICHAEL A.
09017719	5825169	250	02/04/1998	DYNAMICALLY BIASED CURRENT GAIN VOLTAGE REGULATOR WITH LOW QUIESCENT POWER CONSUMPTION	SORNA, MICHAEL A.
10915790	Not Issued	93	08/11/2004	METHODS AND ARRANGEMENTS FOR LINK POWER REDUCTION	SORNA, MICHAEL ANTHONY
08740811	5805088	150	11/01/1996	HIGH SPEED ASYNCHRONOUS SERIAL TO PARALLEL DATA CONVERTER	SORNA, MICHAEL ANTHONY

Inventor Search Completed: No Records to Display.

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Last Name	First Name	
SORNA	MICHAEL	Search

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Inventor Name Search Result

Your Search was:

Last Name = ZIER
First Name = STEVEN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10250043	6937054	150	05/30/2003	PROGRAMMABLE PEAKING RECEIVER AND METHOD	ZIER, STEVEN J.
10711713	Not Issued	41	09/30/2004	High Speed Multi-Mode Receiver	ZIER, STEVEN J.
10905436	7205830	150	01/04/2005	ANALOG MOS CIRCUITS HAVING REDUCED VOLTAGE STRESS	ZIER, STEVEN J.
11163688	7332956	150	10/27/2005	METHOD TO AVOID DEVICE STRESSING	ZIER, STEVEN J.
11203860	7268624	150	08/15/2005	DIFFERENTIAL AMPLIFIER OFFSET VOLTAGE MINIMIZATION INDEPENDENTLY FROM COMMON MODE VOLTAGE ADJUSTMENT	ZIER, STEVEN J.
11272589	7265696	150	11/10/2005	METHODS AND APPARATUS FOR TESTING AN INTEGRATED CIRCUIT	ZIER, STEVEN J.
11383821	Not Issued	41	05/17/2006	Signal Detector with Calibration Circuit Arrangement	ZIER, STEVEN J.
11467349	Not Issued	41	08/25/2006	CML TO CMOS SIGNAL CONVERTER	ZIER, STEVEN J.
11668137	Not Issued	30	01/29/2007	CMOS DIFFERENTIAL RAIL-TO-RAIL LATCH CIRCUITS	ZIER, STEVEN J.
11769128	Not Issued	30	06/27/2007	TRANSMITTER BANDWIDTH OPTIMIZATION CIRCUIT	ZIER, STEVEN J.
11964894	Not Issued	19	12/27/2007	AVOIDING DEVICE STRESSING	ZIER, STEVEN J.
11982206	Not Issued	20	10/31/2007	Design structure for CMOS differential rail-to-rail latch circuits	ZIER, STEVEN J.
11985963	Not Issued	20	11/19/2007	Structure for transmitter bandwidth optimization circuit	ZIER, STEVEN J.
07026229	4746817	150	03/16/1987	BIFET LOGIC CIRCUIT	ZIER, STEVEN J.
07659404	5166552	150	03/08/1991	MULTI-EMITTER BICMOS LOGIC CIRCUIT FAMILY WITH	ZIER, STEVEN J.

				SUPERIOR PERFORMANCE	
09761526	6528777	150	01/16/2001	OPTICAL POWER METER DERIVED FROM COMMON-MODE VOLTAGE OF OPTICAL TRANSIMPEDANCE AMPLIFIER	ZIER, STEVEN JOHN

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